AMENDMENT

In the claims:

Please amend claim 26 as follows.

26. (Four Times Amended) An integrated circuit SRAM cell formed in a semiconductor substrate, a plurality of active transistor regions being formed in the substrate, the SRAM cell comprising:

a first conductive layer disposed on the semiconductor substrate, the first conductive layer forming a plurality of respective control nodes for respective transistors in the substrate;

a second conductive layer disposed over the first conductive layer, the second conductive layer being coupled to the first conductive layer and to active transistor regions to interconnect groups of transistors and thereby form respective data latches;

an interlevel dielectric disposed on the second conductive layer and including three different insulating layers, two of the three insulating layers being independently planarized spin-on glass layers;

an insulating layer disposed on the interlevel dielectric; and

a third conductive layer formed on the insulating layer, the third conductive layer being coupled to the data latches to form respective resistive loads for the respective latches.